NLO 300891 US.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 425 965 A2**

(12) # EUROPEAN PATENT APPLICATION

(21) Application number: **90120230.9**

(22) Date of filing: **22.10.90**

(51) Int. Cl.5: **H01L 21/76**, H01L 21/38

(30) Priority: **03.11.89 US 431420**

(43) Date of publication of application:
08.05.91 Bulletin 91/19

(84) Designated Contracting States:
DE FR GB IT

(71) Applicant: **MOTOROLA INC.**
1303 East Algonquin Road
Schaumburg Illinois 60196(US)

(72) Inventor: **Vasquez, Barbara**
203 E. Redfield Road
Chandler, Arizona 85225(US)
Inventor: **Zdebel, Peter J.**
1720 E. Hale
Mesa, Arizona 85203(US)

(74) Representative: **Ibbotson, Harold et al**
MOTOROLA European Intellectual Property Operations Jays Close Viables Ind. Estate Basingstoke Hants RG22 4PD(GB)

(54) **Method of fabricating semiconductor structures.**

(57) A method of fabricating a semiconductor structure includes forming a thermal oxide layer (12), a polysilicon layer (16) and a first dielectric layer (16,18) on a substrate (10) and using a mask (20) to form at least one opening (22) therein. Dielectric spacers (24) are then formed in the opening (22) and a trench (26) having a self-aligned reduction in width due to the dielectric spacers (24) is etched into the substrate (10) beneath the opening (22). A dielectric trench liner (28) is then formed prior to filling the trench with polysilicon (32). A second mask (36) is then used to form isolation element openings (38) in the first dielectric layer (16) in which shallow isolation elements (40) are formed.

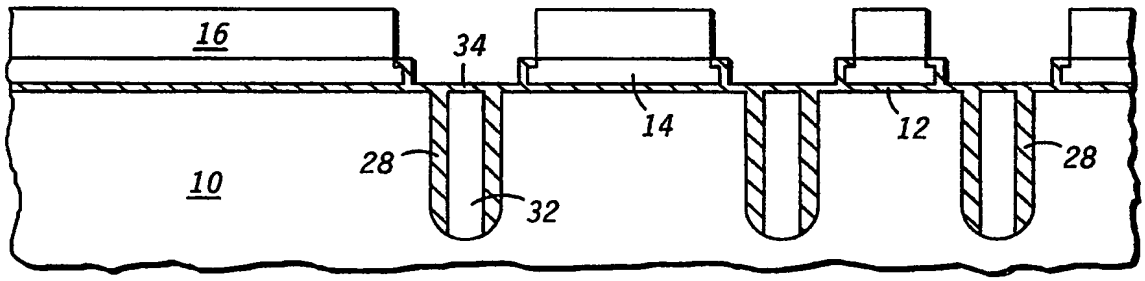

FIG. 12

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METHOD OF FABRICATING SEMICONDUCTOR STRUCTURES

Background of the Invention

This invention relates, in general, to semiconductor devices, and more particularly to a method of fabricating a semiconductor structure that is compatible with multiple technologies.

In the semiconductor art, a trend is toward the fabrication of device structures that are compatible with multiple technologies. For example, structures allowing for the implementation of both bipolar and MOS devices in a single integrated circuit are highly desirable because the best characteristics of both technologies may be obtained. This allows for the fabrication of CMOS and BIMOS high performance integrated circuits. For fabrication methods of multiple technology integrated circuits to become practical, process integration flexibility must be obtained. Additionally, it is desirable to be able to develop methods of fabrication having enhanced scalability characteristics.

Prior art methods of fabricating semiconductor structures having variable width shallow isolation elements, especially those disposed over deep trench isolation elements generally require multiple masking steps. Specifically, masks are used to define the encroachment of the isolation elements into the active regions. Inherent with multiple masking steps are misalignment tolerances that must be provided for. These misalignment tolerances prohibit aggressive scaling of structures and require additional real estate.

Summary of the Invention

Accordingly, the present invention seeks to provide a method of fabricating a semiconductor structure that is compatible with several technologies.

In accordance with the present invention there is provided a method of fabricating a semiconductor structure comprising the steps of:
providing a semiconductor substrate;
forming a thermal oxide layer on said substrate;
forming a polycrystalline semiconductor layer on said thermal oxide layer;
forming a first dielectric layer on said polycrystalline semiconductor layer; the invention being characterized by:
forming a first mask on said first dielectric layer and using said first mask to form at least one opening in said first dielectric layer, said at least one opening extending to said polycrystalline semiconductor layer;
forming dielectric spacers in said at least one opening;
forming a trench in said substrate beneath said at least one opening, said dielectric spacers creating a self-aligned reduction in the width of said trench;
forming a dielectric trench liner in said trench and in said at least one opening;
filling said trench with polycrystalline semiconductor material; and
forming a shallow dielectric isolation element on said filled trench.

Embodiments of the present invention advantageously provide a method of fabricating a semiconductor structure having increased integration flexibility, enhanced scalability characteristics and wherein both deep trench isolation elements and shallow dielectric isolation elements may be fabricated at variable widths. Such a semiconductor structure that may be employed in conjunction with high performance integrated circuits.

Brief Description of the Drawings.

FIGS. 1-16 are highly enlarged cross-sectional views of a portion of a semiconductor structure during processing in accordance with an embodiment of the invention; and
FIGS. 17-18 are highly enlarged cross-sectional views of a portion of a semiconductor structure prior to active device formation in accordance with another embodiment of the invention.

Detailed Description of the Invention

FIGS. 1-16 are highly enlarged cross-sectional views of a portion of a semiconductor structure during processing. It should be understood that the figures herein may not be precisely to scale. Initially, a substrate 10 is provided. In this embodiment, substrate 10 is comprised of monocrystalline silicon however it should be understood that substrates comprising other materials may be used. Depending upon the device application, substrate 10 may comprise semiconductor material wherein pre-isolation processing has been completed to establish required doping profiles and epitaxial layers. A thin thermal oxide layer 12 is formed on substrate 10 followed by the formation of a thin polysilicon layer 14 thereon, preferably by deposition. As one skilled in the art will understand, polysilicon layer 14 will serve as a buffer for the

local oxidation which will be explained presently. A nitride layer 16 is formed on polysilicon layer 14. Nitride layer 16 is formed by CVD in this embodiment although other well known methods may be employed. An oxide layer 18 is then formed, preferably by CVD, on nitride layer 16.

Following the formation of oxide layer 18, a photoresist mask 20 is formed thereon. The formation of photoresist mask 20 includes patterning a photoresist layer by methods well known in the art. Mask 20 is employed to form openings 22 that extend through oxide layer 18 and nitride layer 16 and stop on polysilicon layer 14 as shown in FIG. 2. Openings 22 are formed by reactive ion etching. Once openings 22 have been formed, photoresist mask 20 is removed by a standard photoresist clean.

As shown in FIG. 3, dielectric spacers 24 are formed in openings 22. Spacers 24 are comprised of oxide in this embodiment although nitride or oxynitride may be employed. Oxide spacers 24 are formed by depositing, either by CVD or PECVD, an oxide layer (not shown) and then reactive ion etching the oxide layer to form oxide spacers 24. It should be understood that this oxide spacer etch stops on polysilicon layer 14. Spacers 24 allow for a self-aligned reduction in the widths of openings 22. It should be understood that the use of spacers 24 allows openings 22 to be reduced to widths smaller than those obtainable using conventional photolithography techniques. Further, the width of spacers 24 may be varied according to the application. This enhances scalability characteristics of the structure.

FIG. 4 illustrates the formation of trenches 26 beneath openings 22. Reactive ion etching is employed to form trenches 26. As shown, trenches 26 extend into substrate 10. The width of trenches 26 is determined by the width of the corresponding opening 22 and spacers 24 disposed therein. Although FIGS. 1-4 show a series of trenches 26 of approximately the same width, it should be understood that the present invention may be employed in structures having trenches 26 of varying widths as shown in FIG. 5.

As shown in FIG. 6, a trench clean is performed following the formation of trenches 26. In this embodiment, a dilute solution of hydrofluoric acid is employed to remove sidewall passivation material left in trenches 26 by the reactive ion etch. The trench clean can also be employed to remove oxide spacers 24. Although spacers 24 are shown to be completely removed in this embodiment, partial removal thereof is also possible. The width of spacers 24 to be removed is dependent upon the clean and application for which the structure will be employed.

The removal of spacers 24 exposes the portions of polysilicon layer 14 disposed beneath. This creates a self-aligned offset between the sidewall of trench 26 and the edge of nitride layer 16 which will serve as a mask for the formation of shallow dielectric isolation elements. If spacers 24 comprise nitride or oxynitride, they are not removed at this point and will later serve to minimize the lateral encroachment during shallow isolation element formation as will be explained presently.

FIG. 7 illustrates the formation of a trench liner 28. In this embodiment, trench liner 28 is formed by thermally oxidizing the walls of trench 26. Following the formation of trench liner 28, dielectric material 30 is formed to add thickness to trench liner 28 as shown in FIG. 8.

If contact of trench fill material 32 (see Fig. 9) to substrate 10 is desired in the specific application for which the structure is to be employed, trench liner 28 may be removed from the bottom of trench 26. In this embodiment, trench liner 28 and material 30 are removed from the bottom of trench 26 by anisotropic reactive ion etching. Once trench liner 28 and material 30 have been removed from the bottom of trench 26, the optional implant of a channel stop (not shown) may be performed. Again, this is specific to the application for which the structure is being used.

FIGS. 9 and 10 depict two different embodiments of the present invention wherein trenches 26 are filled with trench fill material 32. In these embodiments, trench fill material 32 comprises polysilicon which may be formed by LPCVD or selective polysilicon growth (SPG). If LPCVD is employed to form polysilicon trench fill 32, it might be necessary to employ a sacrificial material layer and an RIE planarization etchback so that trench fill material 32 is planarized. If SPG is employed, a planarization etchback will not be required. Preferably, the top of trench fill material 32 will be coplanar with the top surface of substrate 10.

Following the formation of polysilicon trench fill 32 and the etchback planarization if necessary, oxide layer 18 is removed to expose nitride layer 16 as shown in FIG. 11. Oxide layer 18 is removed by a wet etch employing dilute hydrofluoric acid in this embodiment although reactive ion etching or various combinations of etches may be employed. In addition to removing oxide layer 18, this etch also removes the spacers resulting from the formation of material 30 that project above polysilicon layer 14 as well as a portion of trench liner 28. Again, it should be understood that if spacers 24 were comprised of oxide and not earlier removed, their removal may occur at this point.

Once the oxide etch has taken place, a dielectric cap 34 comprised of oxide in this embodiment is formed on polysilicon trench fill 32 as shown in FIG. 12. Oxide cap 34 combines with trench liner

28 to essentially seal polysilicon trench fill material 32. Oxide cap 34 is formed by thermally oxidizing polysilicon trench fill 32 and must be thick enough to withstand unmasked reactive ion etching of nitride layer 16 as will be explained presently. Additionally, the exposed edges of polysilicon layer 14 will also be thermally oxidized. It should be understood that the formation of oxide cap 34 is not mandatory.

FIG. 13 illustrates the formation of a mask 36. This occurs by forming a photoresist layer on the structure and then patterning it by methods well known in the art. As shown in FIG. 14 openings 38 are formed in nitride layer 16 using mask 36. Once openings 38 have been formed by methods such as reactive ion etching, mask 36 is removed. One of skill in the art will understand that optional channel stops (not shown) may now be formed in substrate 10 beneath openings 38 by methods well known in the art. Openings 38 allow for the formation of shallow isolation elements that will be explained presently.

Once openings 38 have been formed, poly-buffered LOCOS oxidation occurs in openings 38 and also in the areas where nitride layer 16 was originally removed during the formation of openings 22 to form a series of shallow isolation elements 40. Shallow isolation elements such as 40A may be formed between multiple trenches or may be formed as separately defined shallow isolation elements 40B as shown in FIG. 15. It is also possible to form separate shallow isolation elements 40C over single trenches. FIG. 16 illustrates the formation of shallow isolation elements in the embodiment of the present invention having trenches of varying widths.

The encroachment into active areas by shallow isolation elements 40C formed over trench isolation elements is self-aligned to the edges of nitride layer 16 in openings 22 (see FIG. 2) defined by photoresist mask 20. This results in the encroachment requiring less proportional area and increases the scalability characteristics of the structure.

FIGS. 17-18 are highly enlarged cross-sectional views of two embodiments of a portion of a semiconductor structure prior to active device formation. Once shallow isolation elements 40 have been formed, an active area strip is performed. This strip includes using a wet etch to remove nitride layer 16, polysilicon layer 14 and thermal oxide layer 12 as well as other unwanted materials disposed on the active area.

It should be understood that the present invention may be compatible with multiple technologies and may be employed in high performance integrated circuits. In FIG. 17, the composite shallow isolation element 40 comprising 40A and 40C disposed over and between multiple trenches is ideally suited for bipolar inter-tub isolation while shallow isolation elements 40B are ideally suited for MOS intra-well and bipolar intra-tub isolation. Shallow isolation element 40C disposed over a single trench is ideally suited for densely packed bipolar active areas such as those employed in memory applications and CMOS inter-well isolation. In FIG. 18, shallow isolation elements 40C disposed over variable width trenches may be tailored depending upon the specific application for which they are intended. These variable width trenches allow for increased design flexibility.

To optimize CMOS inter-well isolation, mask 36 (see FIG. 13) may be employed to form shallow isolation elements disposed over and extending beyond the edges of single, variable width trenches. In a BIMOS application, this would create a misregistration between shallow isolation elements in the bipolar regions and those in the MOS regions.

Claims

1. A method of fabricating a semiconductor structure comprising the steps of:
providing a semiconductor substrate (10);
forming a thermal oxide layer (12) on said substrate (10);
forming a polycrystalline semiconductor layer (14) on said thermal oxide layer (12);
forming a first dielectric layer (16,18) on said polycrystalline semiconductor layer (14); the invention being characterized by:
forming a first mask (20) on said first dielectric layer (16,18) and using said first mask (20) to form at least one opening (22) in said first dielectric layer (16,18), said at least one opening (22) extending to said polycrystalline semiconductor layer (14);
forming dielectric spacers (24) in said at least one opening (22);
forming a trench (26) in said substrate (10) beneath said at least one opening (22), said dielectric spacers (24) creating a self-aligned reduction in the width of said trench (26);
forming a dielectric trench liner (28) in said trench (26) and in said at least one opening (22);
filling said trench (26) with polycrystalline semiconductor material (32); and
forming a shallow dielectric isolation element (40) on said filled trench (26).

2. The method of claim 1 wherein the first dielectric layer (16,18) comprises:
a nitride layer (16) formed on the polycrystalline semiconductor layer (14); and
an oxide layer (18) formed on said nitride layer (16).

3. The method of claim 2 further comprising the step of removing the dielectric spacers (24) to create a self-aligned offset between the sidewall of the trench (26) and the edge of the nitride layer (16) to serve as a mask for the formation of the shallow dielectric isolation element (40).

4. The method of claim 2 wherein a dielectric cap (34) is formed on the polycrystalline trench fill (32) and combines with the dielectric trench liner (28) to seal said polycrystalline trench fill (32).

5. The method of claim 4 wherein the oxide layer (18) is removed prior to the formation of the dielectric cap (34).

6. The method of claim 1 wherein the first dielectric layer (16,18), the polycrystalline semiconductor layer (14), and the thermal oxide layer (12) are completely removed following the formation of the shallow dielectric isolation element (40).

7. The method of claim 3 wherein the forming a first mask (20) step includes using said first mask (20) to form a plurality of openings (22) in said first dielectric layer (16,18), the forming dielectric spacers (24) step includes forming dielectric spacers (24) in one or more of said openings (22), the forming a trench (26) step includes forming a plurality of trenches (26) beneath said plurality of openings (22) wherein the width of said plurality of trenches (26) is limited by said dielectric spacers (24) if said dielectric spacers (24) are formed in said openings (22) corresponding to said trenches (26) and the forming a shallow dielectric isolation element (40) step includes forming a shallow dielectric isolation element (40) on one or more of said trenches (26).

8. The method of claim 7 wherein the plurality of trenches (26) are of approximately the same width.

9. The method of claim 7 wherein the plurality of trenches (26) are of varying widths.

10. A method of fabricating a semiconductor structure comprising the steps of:

providing a semiconductor substrate (10);

forming a thermal oxide layer (12) on said substrate (10);

forming a polysilicon layer (14) on said thermal oxide layer (12);

forming a nitride layer (16) on said polysilicon layer (14);

forming an oxide layer (18) on said nitride layer (16);

forming a first mask (20) on said oxide layer (18) and using said first mask (20) to form a plurality of openings (22) extending to said polysilicon layer (14);

forming dielectric spacers (24) in said plurality of openings (22);

forming trenches (26) in said substrate (10) beneath said plurality of openings (22), said dielectric spacers (24) creating a self-aligned reduction in the widths of said trenches (26);

removing said dielectric spacers (24) to expose said polysilicon layer (14) and create a self-aligned offset between the sidewalls of said trenches (26) and the edge of said nitride layer (16);

forming a dielectric trench liner (28) in said plurality of trenches (26);

filling said plurality of trenches (26) with polysilicon (32) so that said polysilicon (32) in said plurality of trenches (26) is substantially planar with said substrate (10);

removing said oxide layer (18) so that said nitride layer (16) is exposed;

forming a second mask (36) on said nitride layer (16) and using said second mask (36) to form isolation element openings (38) in said nitride layer (16); and

forming shallow oxide isolation elements (40) in said isolation element openings (38) and also in those areas where said nitride layer (16) was removed during the formation of said plurality of openings (22), said self-aligned offsets serving to limit the encroachment of said shallow oxide isolation elements (40) formed therebetween.

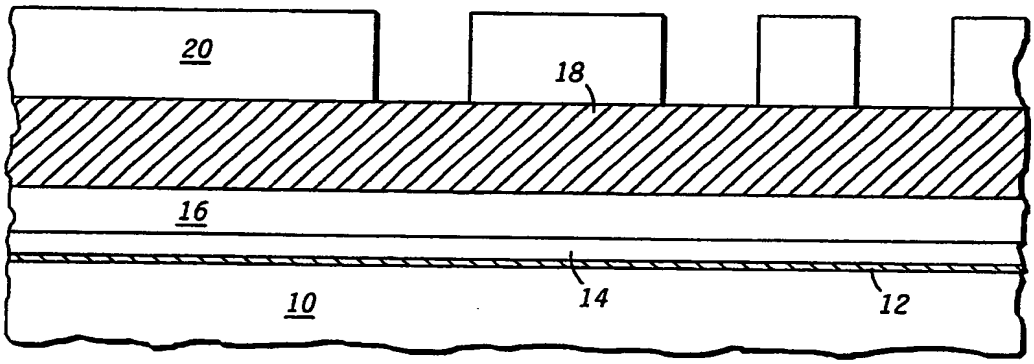

FIG. 1

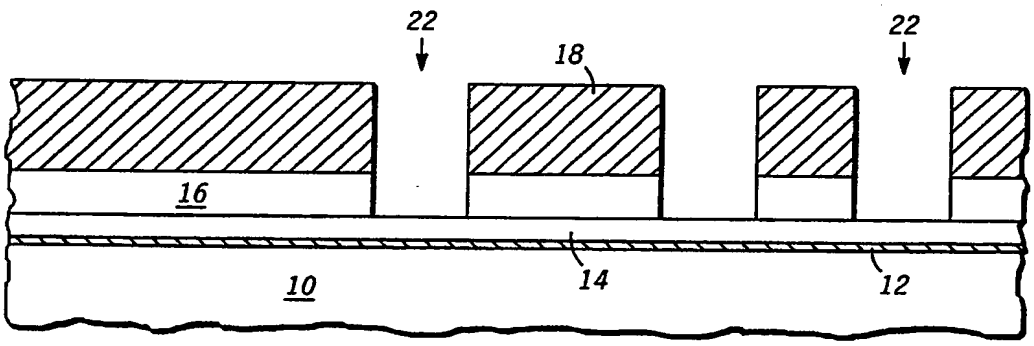

FIG. 2

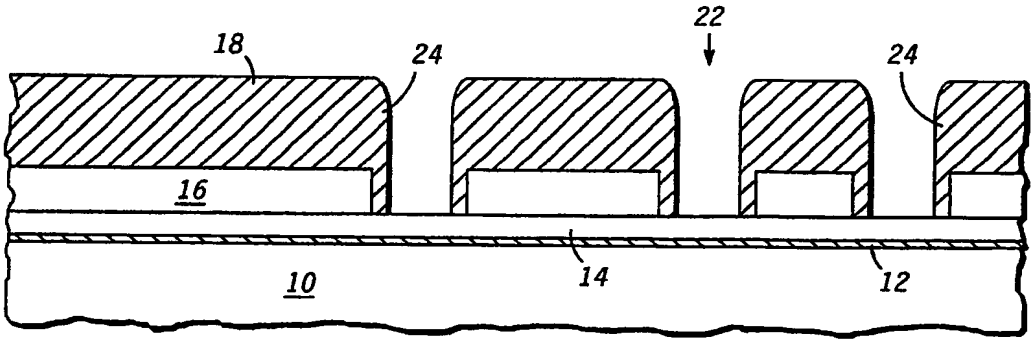

FIG. 3

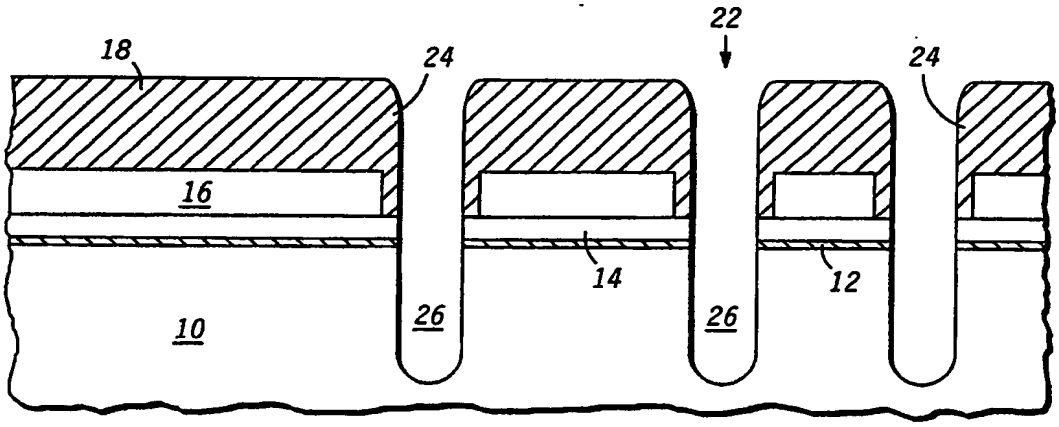

FIG. 4

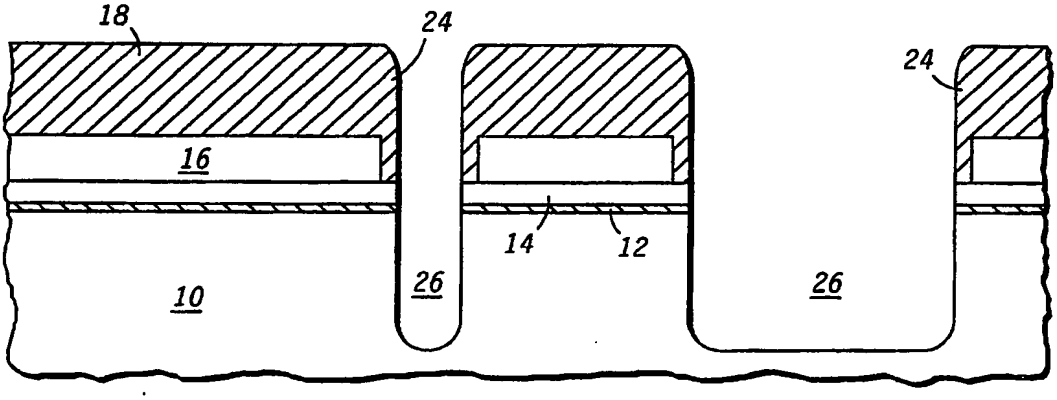

FIG. 5

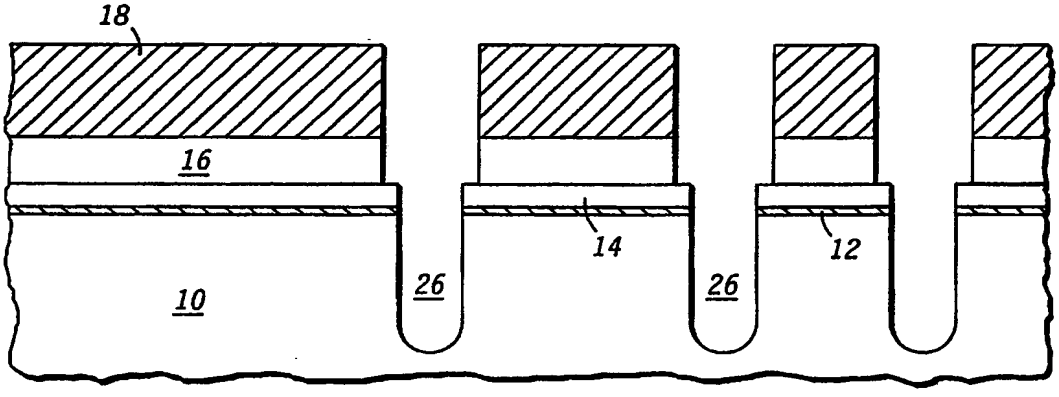

FIG. 6

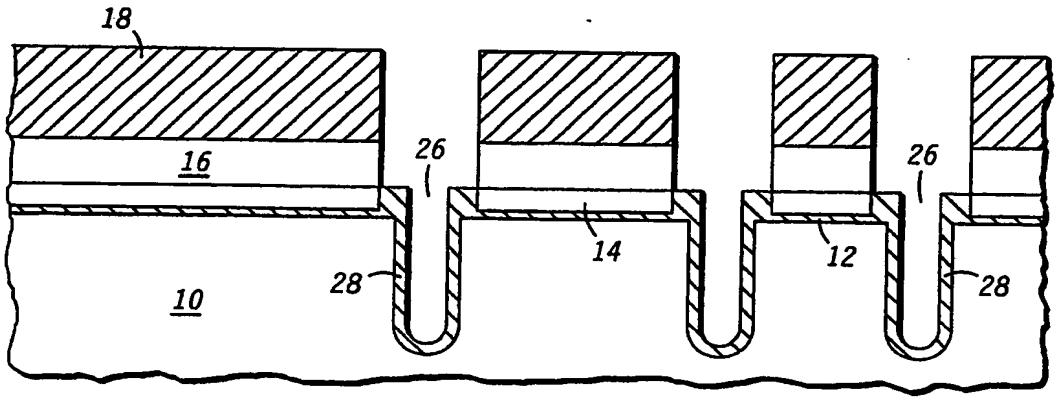

FIG. 7

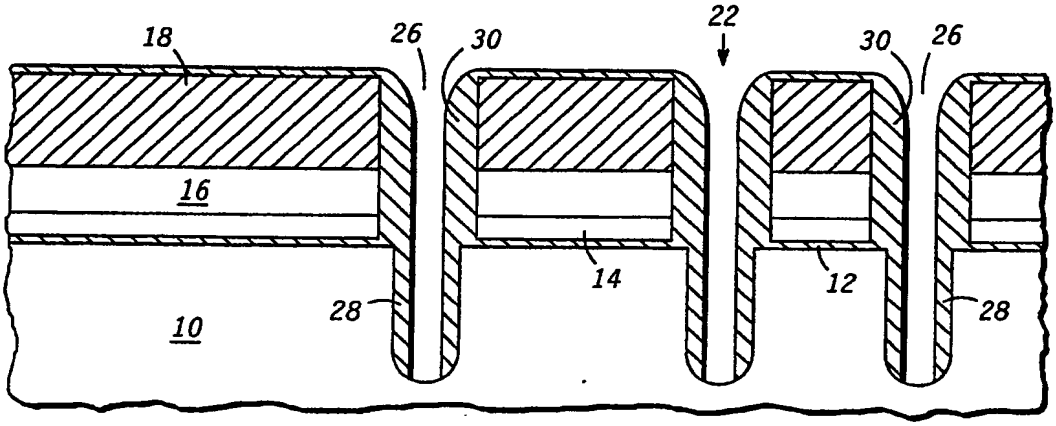

FIG. 8

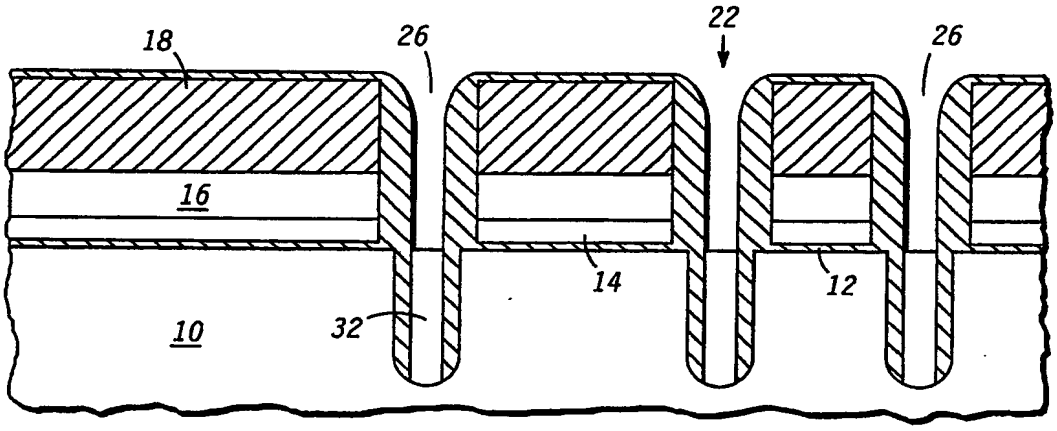

FIG. 9

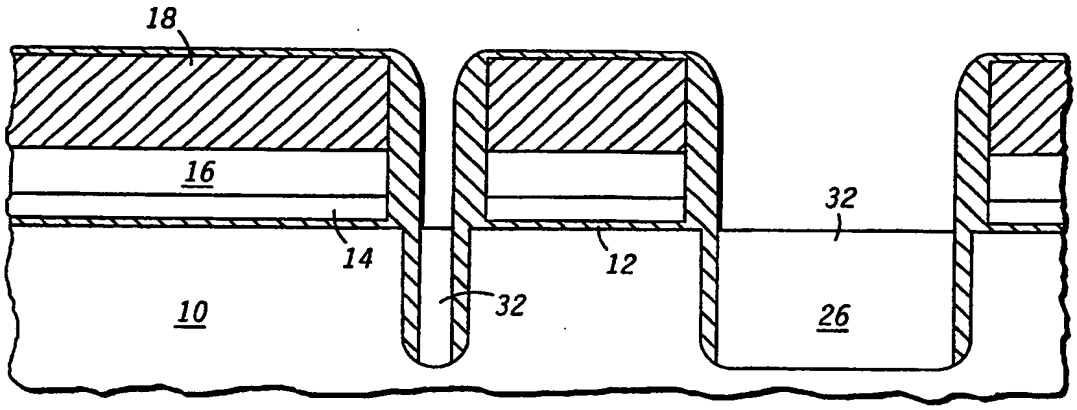

FIG. 10

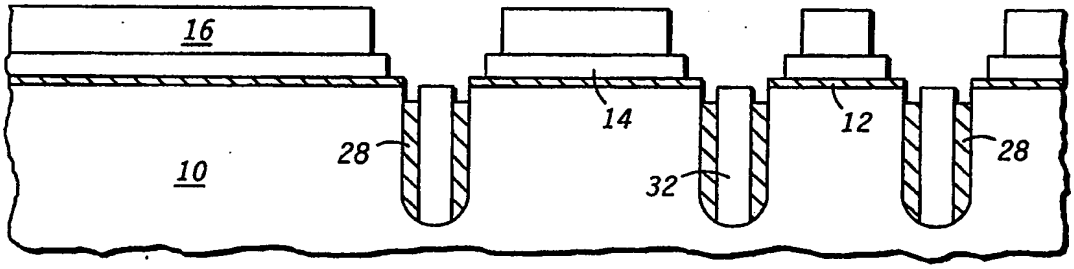

FIG. 11

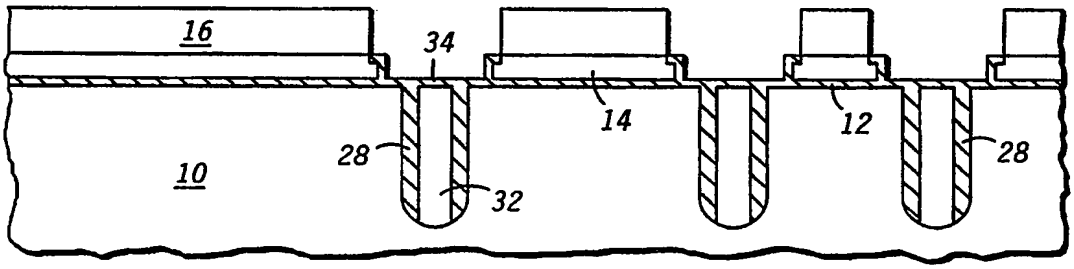

FIG. 12

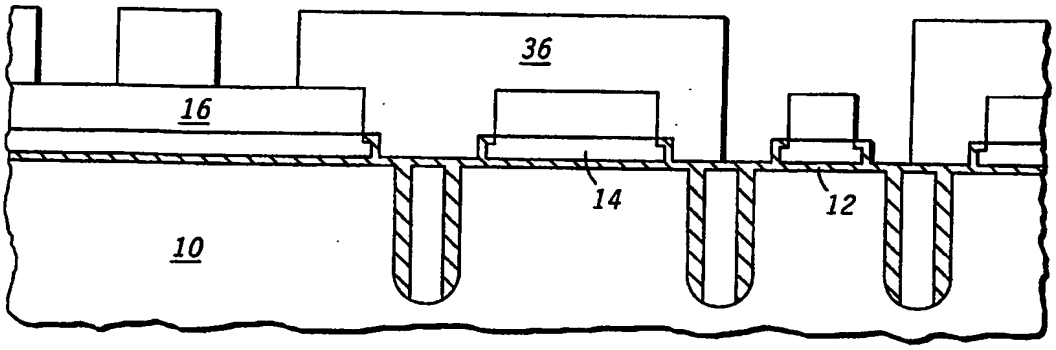

FIG. 13

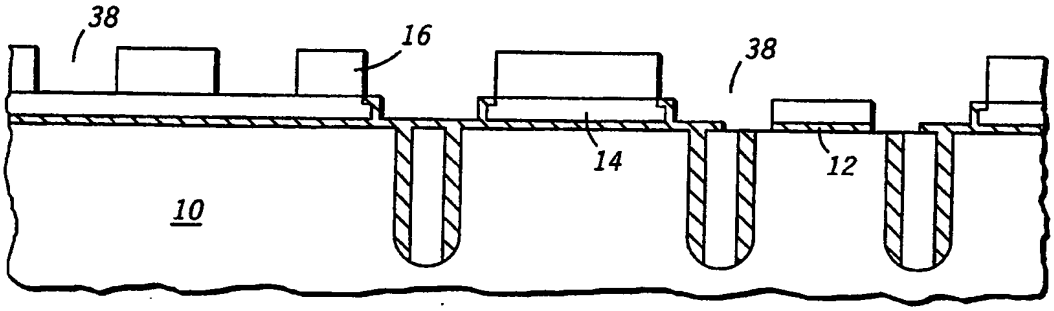

FIG. 14

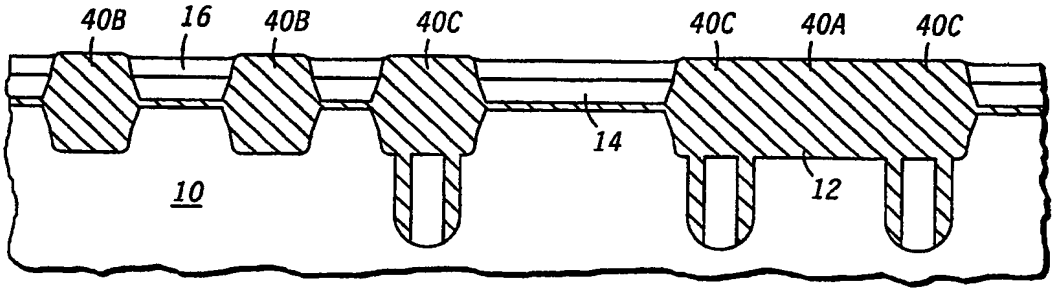

FIG. 15

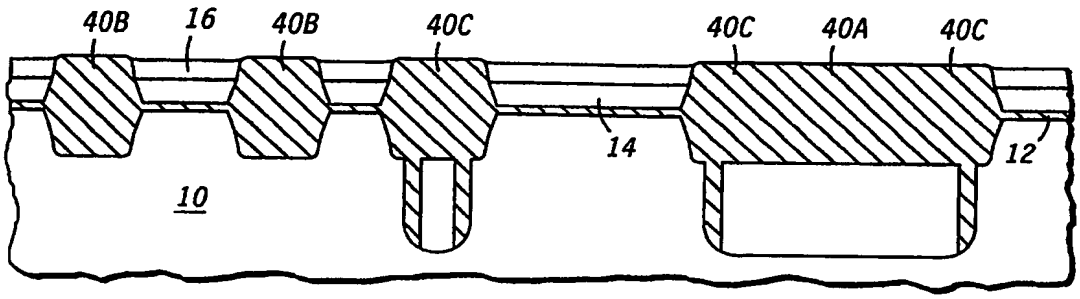

FIG. 16

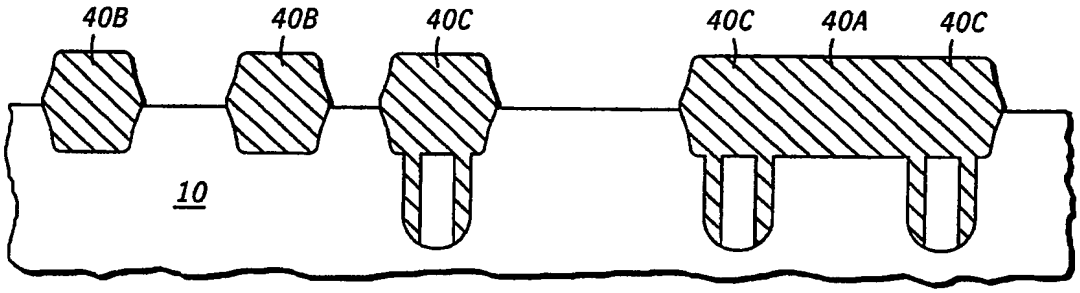

FIG. 17

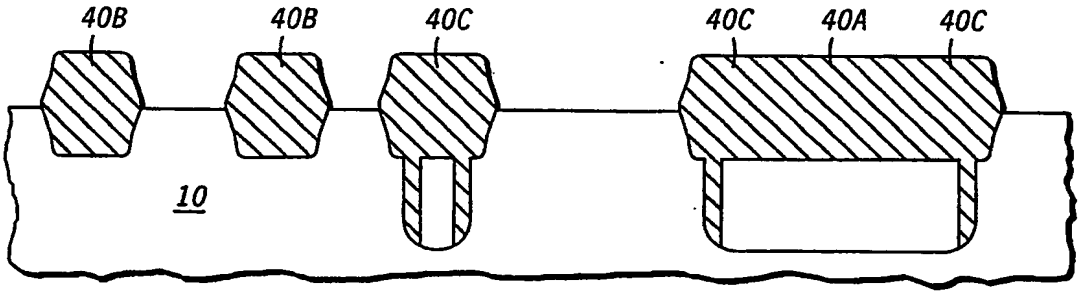

FIG. 18